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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	9

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/489,895	Applicant(s) HENKEL ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12-30-2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-8 have been presented for reconsideration in view of Applicant's arguments and Amended Claim language.

Response to Arguments

2. Applicant's arguments submitted on 12-30-2003 have been fully considered. The Examiner's response is as follows:

2.1 Regarding Applicant's response to the Examiner objecting to the length of the Abstract:

The Applicant has amended the Abstract and the Examiner withdraws any objections to the specification.

2.2 Regarding Applicants arguments concerning the 35 U.S.C. 101 rejections of Claims 6-8:

Applicant argued:

MPEP § 2106(a) states that "... a claimed computer- readable mediun encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory." *See* MPEP § 2106(a), 2'd para. *In re Beauregard,* 35 U.S.P.Q.2d 1385 (Fed. Cir. 1995) held that "computer programs embodied in a tangible medium, such as floppy diskettes, are patentable subject matter under 35 U.S.C. Section 101 and must be examined tinder 35 U.S.C. Sections 102 and 103." Each of claims 6, 7 and 8 recites a computer readable medium that bears computer code embodying the claimed invention. Applicants are not aware of, nor has the Examiner cited, any relevant Federal Circuit case law, Title 37 section or MPEP section that requires a computer product claim to contain language that the computer product must be executed in order to be considered statutory within the ambit of 35 U.S.C. § 101. Applicants respectfully request that the 35 U.S.C. § 101 rejection of claims 6-8 be withdrawn.

The Examiner asserts that, based on a careful reading of Applicant's specification and review of the claim language, the Examiner has determined that the claimed subject matter is

directed towards Functional Descriptive Material, *in this case a computer program,* and therefore Applicant's claims are directed towards statutory subject matter. In view of Applicant's arguments the Examiner withdraws the earlier 35 U.S.C. 101 rejections of Claims 6-8.

2.3 Regarding Applicants response to the 35 U.S.C. 103(a) rejections of Claims 1-2:

Applicant argued:

> The combination of Kageshima and Catthoor *et al.* does not teach or suggest a determination of whether an initially defined instruction set has data dependencies or correlation between instructions, and hence modifying the defined instruction set based on the determination, as recited in claims 1 and 2.

The Examiner asserts that Applicant's arguments are persuasive in that the amended claim language does not teach the limitation of changing the configuration of a core model, *for example changing the buffer on a UART from 4K to 8K*, as disclosed in Applicant's specification, and then re-running the simulation with an interpolated value for the cores new buffer configuration derived from the old power consumption data. The limitation of a UART with different buffer configurations is not positively claimed in the current claim language, *(please see the paragraphs in section 4 of this action.)* However, the Examiner has found Applicants arguments to be persuasive, in that the current prior art of record does not teach or suggest a modified instruction set based on correlated and dependent data, and therefore withdraws the 35 U.S.C. 103(a) rejections of Claims 1-2.

2.4 Regarding the Applicant's arguments regarding the 35 U.S.C. 103 rejection of Claims 3-5:

Applicant argued:

The combination of Kageshima, Catthoor *el al.* and Dean *et al.* does not teach or suggest a determination of whether an initially defined instruction set has data dependencies or correlation between instructions, and thence modifying the defined instruction set based on the determination, as recited in claim 2 and included in claim 3 via dependency. None of the references, either alone or in combination, discloses the refinement of an initially defined instruction set based on the presence of data dependencies or correlation between instructions, as recited in claim 2 and included in claim 3.

The Examiner asserts that Applicant's arguments are persuasive in that the amended claim language does not teach the limitation of changing the configuration of a core model, *for example changing the buffer on a UART from 4K to 8K*, as disclosed in Applicant's specification, and then re-running the simulation with an interpolated power consumption value for the cores new buffer configuration derived from the old power consumption data. The Examiner has found Applicants arguments to be persuasive and withdraws the 35 U.S.C. 103(a) rejections of Claims 3-5.

2.5 Regarding Applicants arguments regarding the 35 U.S.C. 103(a) rejections of Claims 6-8:

Applicant argued:

With respect to claim 6, the combination of Loucks *et al.* and Dean *et al.* falls to teach or suggest at least executable code portions for adding idle energy to an energy accumulator, for calculating consumed power and for adding an energy value to an energy accumulator.

The Examiner asserts that Applicants claim language is so general and vague that the Examiner has reasonably concluded that the claimed limitation could read on a *calculation of consumed power (charging), adding energy (energizing a circuit) and a capacitor (energy accumulator)*, as reading on Applicant's current claim language. Thus, the Examiner can apply a reasonable interpretation on Applicant's claim language to conclude that the Applicant is merely

claiming the modeling of a capacitor charging, *the consumed power being the charge the capacitor is accepting.* The Examiner notes in Applicants specification in figures 5 and 9A and on page 27, *"such that multiple tables of toggle counts or equations for multiple parameter values can be invoked..."* The Examiner asserts that to claim that which is disclosed in the specification the Applicant could amend the current claim language to: *"a third executable code portion for adding an idle energy value to the energy accumulation count;"* The example claim language would clear up any ambiguity in regards to the claim language so as to make the claim language teach away from the limitation of simulating the charge of a capacitor.

Since neither Loucks et al. nor Dean et al. teaches or suggests at least executable code portions for adding idle energy to an energy accumulator, for calculating consumed power and for adding an energy value to an energy accumulator, Applicants believe that one of ordinary skill in the art would not be motivated to combine the references. Although the Examiner provides a motivation analysis with respect to the development of large ASICs with power consumption problems, both Loucks et al. and Dean et al. lack any teaching about the desirability of executable code portions for adding idle energy to an energy accumulator, for calculating consumed power and for adding an energy value to an energy accumulator.

The Examiner asserts that, in Figure 11 of the *Loucks et al.* reference is disclosed the module model used and that there is a "SETUPCOUNTER(C) and UPDATECOUNTER(C)" methods, further, the *Loucks et al.* reference discloses in **Figure 12B** the item labeled "INCREMENT MODULE SETUP COUNTER", further the *Louchs et al.* reference discloses, in **Col. 27 & 28** that there is a counter, that is updated, just like Applicant's toggle counts, which are used, as disclosed in Applicant's specification, to keep track of the energy used during the simulation. After a careful review of Applicant's arguments and the prior art presented in the original Information Disclosure Statement as well as a review of the specification the Examiner asserts that adding an energy value to an energy accumulator is implied in the *Louchs et al.*

reference because the purpose for modeling each element in that reference is for the purpose of power calculation and usage. Applicant's arguments in regards to the 35 U.S.C. 103(a) rejections of Claims 6, 7 & 8 are unpersuasive and the Examiner upholds the rejection of Independent **Claim 6** and withdraws the rejections of **Claims 7 & 8.**

An updated search has revealed new art.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. **Claims 2 and 3** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claims 1-6** of U.S. Patent No. 6,622,287.

A two-way test for obviousness is appropriate in this situation because applicant could not have filed the conflicting claims in a single application, and administrative delay on the part of the Office caused the later filed application to issue first.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the two claims are directed towards determining the power usage of a system of cores with a plurality of functional units.

Specifically, **Claim 1** of U.S. Patent 6,622,287 is directed towards selecting cores that have a low utilization rate *(**Claim 2** of U.S. Application 09/489,895 ...selecting at least one parameterized instruction-based core model...)*, calculating a utilization rate of each of said cores *(**Claim 3** of U.S. Application 09/489,895 ...at the least one parameterized instruction-based core model includes toggle counts for a plurality of implementations of the deployed circuit)*, comparing the utilization rates of the partitioning objects with the utilization rates of the selected cores from which the partitioning objects were extracted *(**Claim 2** of U.S. Application 09/489,895 ...a refined instruction set derived from captured gate-level energy simulation data)*, selecting cores from said set of cores that have a low utilization rate, **Claim 2** further comprising a step of determining said functional units of said cores by examining code segments that make up a set of operations of said cores, *(**Claim 1** of U.S. Application 09/489,895...analyzing the estimated energy requirements of the circuit model)*.

It would have been obvious, to an artisan of ordinary skill, to have used the partitioning methods, as disclosed in U.S. Patent 6,622,287, in **Claims 1-6** to model the power consumption of different core elements of a System On a Chip or SOC as disclosed in **Claims 2 & 3** of U.S. Patent Application 09/489,895 because, the modeling methodology for the partitioned objects based on utilization is also used to determine power usage, which depends on the configuration of the core being modeled and the type of activity being performed by the core when the power consumption may is being determined, **(U.S. Patent 6,622,287 Col. 2 Lines 6-24).**

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-8 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4.1 In independent **Claim 1** the Applicant claims, *capturing gate-level energy simulation data wherein the captured gate-level data simulation data correlates to an initially defined instruction set.* The Examiner notes that Applicant's specification discloses a method of modeling a core element of a System On a Chip (SOC) and then performing a complex simulation and tracking the energy consumption of the modeled core element in a set configuration, extrapolating what the power consumption would be for that core element if the configuration was changed, *for example a UARTs buffer is increased in size,* and then based on the data collected from the original simulation, a new simulation is run, at a higher level of abstraction, using the extrapolated energy consumption data derived from the earlier complex simulation. The use of the term *"instruction set"* is teaching away from the actual invention as disclosed in Applicants specification *(see pages 36-40 & all of the figures)* in which there are described lower level models and higher level models and the Examiner does not detect any of that language, in the current claim language.

In another section of amended **Claim 1** the Applicant states: *"determining if no data dependencies or no correlation between instructions of the initially defined instruction set are present, and if so, increasing the complexity of the initially defined instruction to create a refined instruction set:"*

The Examiner asserts that the following Claim language would clearly claim the limitations as disclosed in Applicant's specification; "*analyzing the model of the core element based on the data collected during the initial complex simulation, where the core element is in an initial configuration and then determining the amount of energy consumed by the core element when the configuration is changed, extrapolating energy data based on the data collected in the first simulation, so that it can be used at a higher level of abstraction in a new simulation to determine power consumption*".

4.2 In independent **Claim 2** the Applicant claims, *"a refined instruction set derived from captured gate-level energy simulation data, wherein the captured gate-level simulation data is correlated to an initially defined instruction set, and the complexity of the initially defined instruction set has been increased or decreased on the basis of the presence of data dependencies or correlation between instructions of the initially defined instruction set to form a refined instruction set;"* The Examiner asserts that Applicant's specification is directed towards refining a model and not refining an instruction set.

The Examiner asserts that the following Claim language would clearly claim the limitations as disclosed in Applicant's specification; *"a refined model derived from gate-level energy usage simulation data, where the captured gate-level simulation data is correlated to an initially configured circuit model, and the complexity of the initially defined circuit model has been increased or decreased on the basis of the current configuration data of the circuit device being modeled and interpolating new energy usage data using derived simulation data which was based on the original complex simulation model."*

4.3 In independent **Claim 4** the Applicant claims, *"determining if no data dependencies or no correlation between instructions of the plurality of high-level instructions are present, and if so, increasing the complexity of the plurality of high-level instructions to create a refined instruction set;"* The Examiner asserts that Applicant's specification is directed towards refining a model and not refining an instruction set.

The Examiner asserts that the following Claim language would clearly claim the limitations as disclosed in Applicant's specification; *"increasing the complexity of the model, so that the initial energy consumption data derived from a simulation of a model with an initial configuration will not propagate a greater degree of error, when the simulation data is used to extrapolate a new model which will reflect a different configuration of the device being simulated."*

4.4 In Independent **Claim 6** the Applicant claims, *"a third executable code portion for adding an idle energy value to an energy accumulator;"* The Examiner can apply a reasonable interpretation on Applicant's claim language to conclude that the Applicant is merely claiming the modeling of a capacitor charging, *the consumed power being the charge the capacitor is accepting.* The Examiner notes in Applicants specification in figures 5 and 9A and on page 27, *"such that multiple tables of toggle counts or equations for multiple parameter values can be invoked..."* The Examiner asserts that to claim that which is disclosed in the specification the Applicant could amend the current claim language to: *"a third executable code portion for adding an idle energy <u>value</u> to the energy accumulation <u>count</u>;"* The example claim language would clear up any ambiguity in regards to the claim language so as to make the claim language teach away from the limitation of simulating the charge of a capacitor.

4.5 In independent **Claim 7** the Applicant claims, *"Wherein the simulated instruction is from a refined instruction set derived from captured gate-level energy simulation data..."* The Examiner asserts that this claim language is teaching away from the Applicant's specification. The Examiner asserts that the following Claim language would clearly claim the limitations as disclosed in Applicant's specification; *"Wherein the model being simulated is a model derived from another model of the same core device, that had a different configuration, and this new refined core model had its energy consumption rate data derived from the energy consumption rate data of the complex simulation of the original model."*

4.6 In independent **Claim 8** the Applicant claims, *"the parameterized core model comprises a refined instruction set associated with the at least one member function and derived from captured gate-level energy simulation data, wherein the captured gate-level data simulation data is correlated to an initially defined instruction set"*. The Examiner asserts that this claim language is teaching away from the Applicant's specification in that the proposed invention is directed towards a refined *model* and not a refined *instruction set.* The Examiner asserts that the following Claim language would clearly claim the limitations as disclosed in Applicant's specification; *"the parameterized core model comprises a refined data set derived from captured gate-level energy simulation data of the model in an initial configuration, wherein the refined gate-level simulation data is derived from the initial parameterized core models energy simulation data, when the core model was in its initial configuration"*.

4.7 Claim 6 recites the limitation "the energy accumulator" in last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Independent **Claims 1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kageshima U.S. Patent 6,096,089** in view of **Catthoor et al. U.S. Patent 6,223,274** and in further view of **Allen et al. U.S. Patent 6,151,568.**

5.1 As regards independent **Claims 1 and 2** the *Kageshima* reference discloses a method of power estimation of a core-model **(Figure 1),** capturing gate-level simulation data **(Figure 2),** deploying the captured gate-level simulation data where this data correlates to a plurality of instructions to obtain power estimations for each instruction **(Figure 11).**

However, the *Kageshima* reference does not expressly disclose an embedded system or system-on-a-chip.

The *Catthoor et al.* reference discloses a method of calculating the energy consumption of an embedded system or system-on-a-chip **(Figures 4, 6, 16, 20, Col. 3 Lines 49-53, Col. 5 Lines 54-59).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Catthoor et al.* reference because of the problems in industry related to the development of fast video chips that are also power efficient. Large ASICs with on-board embedded processors consume a great deal of energy and it is important for portable device, such as laptops, to be energy efficient so that they will not exhaust their limited supply of battery power **(*Catthoor et al.*, Col. 2 Lines 1-16).**

The *Kageshima* reference does not expressly disclose, *determining if no data dependencies or no correlation between instructions of the initially defined instruction set are present, and if so, increasing the complexity of the initially defined instruction to create a refined instruction set.*

The *Allen et al.* reference discloses refining a power estimation of a model **(Figure 1 Item 16, Figure 2 Item 76, Figures 5 & 6, Col. 4 Lines 35-42, Col. 4 Lines 57-67 and Col. 5 Lines 1-3, Col. 5 Liens 10-17).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the power estimation technologies of the *Kageshima* reference with the refining or a power estimating technology of the *Allen et al.* reference because, during a design an artisan might want to determine how a particular core element in a SOC design might perform if it is configured in a different manner **(Allen et al. Col. 2 Lines 20-23).**

6. Dependent **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kageshima U.S. Patent 6,096,089** in view of **Catthoor et al. U.S. Patent 6,223,274** and in further view of **Allen et al. U.S. Patent 6,151,568** and in further view of **Dean et al. U.S. Patent 6,397,170.**

6.1 As regards independent **Claim 2** see paragraph **5.1** above.

6.2 As regards dependent **Claim 3** the *Kageshima* reference does not expressly disclose toggle counts in a power estimation simulator.

The *Dean et al.* reference discloses toggle counts in a power estimation simulator **(Figure 1).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Dean et al.* reference because by including the toggle counts in the power estimation the power calculation be come more accurate **(Dean et al. Col. 2 Lines 7-20).**

7. Independent **Claim 4** and dependent **Claim 5** are being rejected under 35 U.S.C. 103(a) as being unpatentable over **Kageshima U.S. Patent 6,096,089** in view of **Catthoor et al. U.S. Patent 6,223,274** and in further view of **Dean et al. U.S. Patent 6,397,170** in further view of **Allen et al. U.S. Patent 6,151,568.**

7.1 As regards independent **Claim 5** the *Kageshima* reference discloses a method of power estimation of a core-model **(Figure 1),** capturing gate-level simulation data **(Figure 2),** deploying the captured gate-level simulation data where this data correlates to a plurality of instructions to obtain power estimations for each instruction **(Figure 11).**

However, the *Kageshima* reference does not expressly disclose an embedded system or system-on-a-chip.

The *Catthoor et al.* reference discloses a method of calculating the energy consumption of an embedded system or system-on-a-chip **(Figures 4, 6, 16, 20, Col. 3 Lines 49-53, Col. 5 Lines 54-59).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Catthoor et al.* reference because of the problems in industry related to the development of fast video chips that are also power efficient. Large ASICs with on-board embedded processors consume a great deal of energy and it is important for portable device, such as laptops, to be energy efficient so that they will not exhaust their limited supply of battery power **(*Catthoor et al.*, Col. 2 Lines 1-16).**

The *Kageshima* reference does not expressly disclose refining a model with interpolated energy consumption values derived from an earlier complex simulation.

The *Allen et al.* reference discloses refining a power estimation of a model **(Figure 1 Item 16, Figure 2 Item 76, Figures 5 & 6, Col. 4 Lines 35-42, Col. 4 Lines 57-67 and Col. 5 Lines 1-3, Col. 5 Liens 10-17).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the power estimation technologies of the *Kageshima* reference with the refining or a power estimating technology of the *Allen et al.* reference because, during a design an artisan might want to determine how a particular core element in a SOC design might perform if it is configured in a different manner **(Allen et al. Col. 2 Lines 20-23).**

7.2 As regards dependent **Claim 5** the *Kageshima* reference does not expressly disclose using a hardware description language.

The *Dean et al.* reference discloses a hardware description language **(Col. 2 Lines 21-37).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Dean et al.* reference because, HDL's are used to model modern VHLIC circuit designs and therefore an artisan in the circuit design area is required to know how to design using these design tools **(Dean et al. Col. 2 Lines 65-67, Col. 3 Lines 1-10).**

8. Independent **Claims 6, 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Loucks et al. U.S. Patent 5,828,576** in view of **Catthoor et al. U.S. Patent 6,223,274.**

8.1 As regards independent **Claims 6, 7 and 8** the *Loucks et al.* reference discloses an object oriented method of modeling a circuit design for the purpose of monitoring power consumption **(Figures 5A-5L, 10, 10A, 10B, 10C, 11, Col. 3 Lines 60-67, Col. 4 Lines 1-35).**

However, the *Loucks et al.* reference does not expressly disclose simulating an embedded system or system-on-a-chip.

The *Catthoor et al.* reference discloses a method of calculating the energy consumption of an embedded system or system-on-a-chip **(Figures 4, 6, 16, 20, Col. 3 Lines 49-53, Col. 5 Lines 54-59).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Loucks et al.* reference with the *Catthoor et al.* reference

because of the problems in industry related to the development of fast video chips that are also power efficient. Large ASICs with on-board embedded processors consume a great deal of energy and it is important for portable device, such as laptops, to be energy efficient so that they will not exhaust their limited supply of battery power **(*Catthoor et al.*, Col. 2 Lines 1-16).**

8.2 As regards independent **Claims 7 & 8.**

The *Kageshima* reference does not expressly disclose refining a model with interpolated energy consumption values derived from an earlier complex simulation of a core element.

The *Allen et al.* reference discloses refining a power estimation of a model **(Figure 1 Item 16, Figure 2 Item 76, Figures 5 & 6, Col. 4 Lines 35-42, Col. 4 Lines 57-67 and Col. 5 Lines 1-3, Col. 5 Liens 10-17).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the power estimation technologies of the *Kageshima* reference with the refining or a power estimating technology of the *Allen et al.* reference because, during a design an artisan might want to determine how a particular core element in a SOC design might perform if it is configured in a different manner **(Allen et al. Col. 2 Lines 20-23).**

Conclusion

9. An updated search has revealed new art. **Claims 1-8** have been reconsidered and rejected. This action is **NON-FINAL.**

9.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC